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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/188,241	Applicant(s) LUO, WENZHE	
	Examiner Terry L Englund	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,18,19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,18,19,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on ____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *14 June 2001* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment/RCE

The amendment submitted on Nov 14, 2001 was entered after the approval and entry of the RCE on Dec 6, 2001. The amendment has now been reviewed and considered with the following results:

The objection of Fig. 4 in the previous Office Action was a typo. Fig. 4 clearly shows "Vo". The objection was actually meant for Fig. 2. Therefore, the objection to "Fig. 4" has been withdrawn.

The amendment's comments indicated the addition of "Vo" to Fig. 2 made the drawing correspond to page 4, line 6. However, that line indicates "Vdd-Vo" is the drain-source voltage of switch MS. It is not the (supply) voltage at the source of MS. Therefore, Fig. 2 should show only VDD at the source of MS, and "Vo" should be shown at the drain of switch MS (i.e. common connection of MS and MC). Also, related to the proposed drawing change, the amendment lacks any good explanation of why power supply VDD (shown in Figs. 1, 2, 4, and 7) was changed to "VDD-Vo" only on Fig. 2. Therefore, Fig. 2 is objected to, and its objection is described later under the appropriate section.

The cancellation of claims 15-17 and 20 rendered their respective rejection moot.

The comments with respect to page 7, lines 17-22 did not satisfactorily address the objection described in the previous Office Action. Therefore, that basic objection has been maintained, and a modified objection is described later under the appropriate section. Related comments are under the Response to Arguments section.

The rejections of claims 21 and 22 under 35 U.S.C. 112, second paragraph are maintained. Modified rejections, taking into account the amended claim changes, are described later under the appropriate section. Related comments are under the Response to Arguments section. Also, other rejections under 35 U.S.C. 112 are described later with respect to the amended changes within the various claims.

The rejections of: 1) claims 1-5, 8-10, 12, 18, 19, 21, and 22 under 35 U.S.C. 102(e), with respect to Ravon; 2) claims 6, 7, 11, 13 and 14 under 35 U.S.C. 103(a), with respect to Ravon; and 3) claims 1-14, 18 and 19 under 35 U.S.C. 103(a), with respect to Harston are maintained. The rejections are described later under the appropriate section, with modifications to take into account the amended changes. Related comments, with respect to the prior art references, are under the Response to Arguments section.

Specification

The disclosure is objected to because of the following informalities: It is suggested "switch MC" on both lines 18 and 19 of page 7 be changed to --switch MS--. Only then will the description clarify the current levels associated with the current source MC and switch MS shown in the applicant's Fig. 5. Appropriate corrections are required.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claims 1-14, 18, 19, 21 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear in independent claims 1 (line 6), 18 (lines 4-5), 21 (lines 8-9), and 22 (lines 9-10) what "to equalize a current level produced by said current source" means. For example, it is equalized with respect to what? Also, if the current source is providing a constant current, wouldn't that be considered equal to its desired operational current? The relationship between "a current source" in claim 2 (line 3) and "a current source" now recited in claim 1 (line 3) needs clarification. For example, does the applicant now want to include an additional current source not previously disclosed? If the current sources are meant to be the same, the claims should clearly indicate that. Similarly, how does "a current source" of claim 14 (line 3) relate to "a current source" of claim 1?

The description "continuously receives said current flowing from said current source" in claims 21 (lines 10-11) and 22 (lines 11-12) is still considered misleading. For example, the applicant's Fig. 5 shows current IA from current source 420 will flow to load 440 only when transistor switch 430 is conducting. However, when transistor switch 430 is open, current IA cannot flow from the current source to the load. Therefore, how can the load "substantially continuously" receive the current source's current when switch MS is open, and the current is flowing through the pull-down mirror path?

Dependent claims carry over the rejection from their respective independent claim.

Claim Rejections under 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

In so far as being understood, claims 1-5, 8-10, 12, 18, 19, 21, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ravon. For the following descriptions, Figs. 2-4 of Ravon will be considered and/or referred to, wherein one of ordinary skill in the art would be able to recognize the relationships between the figures. In Fig. 2, Ravon shows a current source switching circuit comprising a transistor switch M1; what can be deemed a pull-down mirror path M2,13,14 in parallel with transistor switch M1 (e.g. they are both coupled between terminal E and ground); and first load C'. Current source 11 is shown in detail in Fig. 3 (see column 4, lines 44-45), and is disclosed as providing a constant current I (e.g. see column 3, line 31). Fig. 4 shows first load C', transistor M2, and details of comparator 14. Although transistor switch M1 is replaced by diode D1 in Fig. 4 (see column 6, lines 16-18), Ravon also discloses a transistor provides better efficiency on column 6, lines 24-25. Therefore, for the following description, diode D1 of Fig. 4 will be replaced with a transistor switch (e.g. M1 of Fig. 2) for improved efficiency, wherein block 13 of Fig. 2 will be used to control the on/off operations of both transistors M1 and M2. One of ordinary skill in the art would recognize that current source 11 (shown in Figs. 2 and 3) provides current I to terminal

E of Fig. 4. Although the reference does not clearly disclose the "substantially continuously" reduction of "charge injection" as recited within the claims, one of ordinary skill in the art would know it relates to the current received by the load capacitor. When transistor M2 is off and transistor switch M1 is on, first load C' receives current I (from current source 11) through transistor switch M1 (e.g. see Fig. 2). Besides charging first load C', the current also charges capacitor C1 through resistor R1 (see Fig. 4). [Note that the structure of first load C', capacitor C1, resistor R1, and amplifier 20 closely corresponds to the respective load 440, capacitor C1, resistor R1, and amplifier 400 structure of the applicant's Fig. 5.] When transistor switch M1 is turned off, and transistor M2 is turned on, capacitor C1 will help maintain the voltage across first load C' (i.e. between terminal S and ground), and less current will be required to completely charge first load C' back up once transistor switch M1 is turned back on. Also, since current I is constant, the current flowing through M2 will be equal to the current flowing through M1, when the respective transistor is conducting. Therefore, transistor switch M1 and pull-down mirror path M2,13,14 substantially continuously reduce the charge injection into first load C', and claim 1 is anticipated. The voltage at terminal S will be basically maintained across first load C' by the voltage held across capacitor C1, when switch M1 is not conducting. Once switch M1 begins to conduct again, current I will flow through switch M1 and into load C' without any abrupt changes of voltage and current. Therefore, charge injection flowing to load C' is reduced. Fig. 2 clearly shows current source 11 connected between power source Vc and a first side (i.e. terminal E) of transistor switch M1, and first load C' connected between ground and a second side

(i.e. terminal S) of transistor switch M1, thus anticipating claims 2 and 3. Since first load C' is a charging capacitor, and transistor M1 is a MOS transistor, claims 4 and 5 are also anticipated. Transistor M2 of the pull-down mirror path M2,13,14 can be deemed a pull-down amplifier, anticipating claim 8. When transistor M2 is conducting, its output (i.e. drain) follows the current source 11 side of the transistor switch M1 by allowing the current to flow through transistor M2, thus claim 9 is anticipated. Transistors M1 and M2 receive their respective signals from control 13 (see Fig. 2) which allows transistor M2 to be turned off, and then transistor M1 to be turned on (see column 4, lines 28-30). Therefore, transistor M2 is deemed a complementary pull-down mirror path transistor switch which operates opposite the transistor switch M1, anticipating claim 10. Since current source 11 comprises MOS transistor M3 (e.g. see Fig. 3), claim 12 is anticipated. Transistor/switch M2 provides a pull-down mirror path parallel with current switch M1 (e.g. coupled between terminal E and ground), wherein switches M2 and M1 are substantially turned on and off alternatively, anticipating 18 and 19 because when transistor M1 is off, the capacitor C1 will basically maintain a voltage on load capacitor C', thus substantially continuously reducing the charge injection flowing to the load while equalizing the current flow (e.g. current I will flow through either M1 or M2, depending on which one is conducting). Transistor switch M1 connects current source 11 to load C', and it is substantially simultaneously turned off when switch M2 is turned on. When switch M2 is on, the current I from current source 11 flows through the pull-down mirror path M2,13,14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C', the charge injection will be reduced when transistor

switch M1 is opened, and claim 21 is anticipated. The upper output of block 13 is coupled to the gate of transistor switch M1 and is deemed the means for opening transistor switch M1, and the lower output of block 13 is coupled to the gate of switch M2 and is deemed the means for closing switch M2, wherein current I from current source 11 flows through the pull-down mirror path M2,13,14. Since capacitor C1, of the pull-down mirror path M2,13,14, helps maintain a voltage across load C', the charge injection will be reduced when transistor switch M1 is opened, and claim 22 is anticipated.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to respective claims 1 and 10 above, and further in view of the applicant's Prior Art Fig. 3. As described previously, the basic current source switching circuit is shown and disclosed by the reference of Ravon. However, the reference does not show or disclose the use of the serial combinations of transistors as recited within claims 6, 7 and 11. Ravon shows only a single transistor for transistor switch M1 and one transistor for complementary pull-down mirror path transistor switch M2. It would have been obvious to one of ordinary skill in the art to replace each of transistors M1 and M2 of Ravon's circuit with a respective compensated transistor switch of the

applicant's Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial combination of respective first compensating, functional MOS, and second compensating transistors, wherein transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/well known means for reducing charge injection. Since Ravon's circuit can be considered a current type switch circuit for charging first load C', the compensated switch of the applicant's Fig. 3 would help reduce charge injection even more within the circuit if that was desired.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ravon as applied to claim 1 above. As described previously, Figs. 2 and 4 of Ravon show a circuit with a transistor switch M1, pull-down mirror path M2,13,14, current source 11, and first load C'. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuitry of Ravon by reversing the polarities (i.e. Vc and ground would be reversed) and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage (e.g. closer to power source Vc). The reversal would replace all the MOS transistors (i.e. M1-M6) with their complementary transistors (i.e. an NMOS transistor would be replaced with a PMOS transistor). In this case, transistor M2 would be coupled between power source Vc and the common connection of current source 11/transistor switch M1, and first load C' would be coupled between power source Vc and terminal S. Therefore, transistor M2 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current

source 11 would be coupled between ground and one side (i.e. terminal E) of transistor switch M1, rendering obvious claim 14.

In so far as being understood, claims 1-5, 8-10, 12, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harston. In Fig. 3 Harston shows a current source switching circuit comprising transistor switch MP2; a pull-down mirror path MP3 in parallel with said transistor switch MP2; and first load 10pf. Although the reference does not clearly disclose a reduction in charge injection, it would be obvious to one of ordinary skill in the art that resistor 37.5Ω would be one means that reduces the charge injection flowing to first load 10pf because it will start discharging first load 10pf when transistor switch MP2 is turned off. For example, when transistor switch MP2 is off, the current from current source MP1 will flow through MP3 to ground. Since the current that flows through MP2 and MP3 is from the same current source, they are deemed equalized. Also, when current is flowing through MP3 (and not MP2), and there is still a charge on first load 10pf, the charge injection flowing to the first load will be substantially continuously reduced, thus rendering claim 1 obvious. [MP3 is considered a pull-down mirror path since it mirrors the operation of the transistor switch MP2 and allows the current from transistor MP1 to flow down to ground when switch MP2 is not conducting. See column 2, lines 64-68.] Fig. 3 also shows a current source MP1 (a MOS transistor) coupled between power source CURRENT CELL and the first side of transistor switch MP2; and load 10pf is a charging capacitor 10pf coupled between ground and a second side of transistor switch MP2, thus rendering obvious claims 2-5. Since a transistor can be deemed an amplifier, pull-down mirror path MP3 can be deemed a pull-down amplifier, rendering claim 8 obvious. When transistor MP3 is conducting, its output (i.e. drain) follows the current source MP1 side of the transistor switch MP2 by allowing the current to flow through transistor MP3, thus rendering

obvious claim 9. Transistors MP2 and MP3 receive their respective signals DATAB and DATA. Therefore, transistor MP3 can be deemed a complementary pull-down mirror path transistor switch operating the opposite of transistor switch MP2, rendering claim 10 obvious. It is complementary since it receives a control signal which is a complement of the signal received by transistor switch MP2. Since current source MP1 is a MOS transistor, claim 12 is rendered obvious. Transistor/switch MP3 provides a pull-down mirror path parallel with current switch MP2, wherein switches MP3 and MP2 are alternatively on and off, rendering obvious claims 18 and 19 because when transistor MP2 is off, the resistor 37.5Ω will discharge load 10pf, thus substantially continuously reducing the charge injection flowing to the load. For example, when the load capacitor is discharging, the current/charge injection will flow away from the load. Therefore, the current/charge injection flowing to the load is continuously reduced when MP2 is not conducting. Also, when MP2 begins conducting before load capacitor 10pf has completely discharged through resistor 37.5Ω, the current (e.g. charge injection) required to charge the load capacitor back up will be less. Therefore, the current/charge injection flowing to the load can still be considered continuously reduced.

Claims 6, 7, and 11 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to claims 1 and 10 above, and further in view of the compensated transistor switch of the applicant's Prior Art Fig. 3. Harston shows only a single transistor for each of transistor switch MP2 and complementary pull-down mirror path transistor switch MP3. It would have been obvious to one of ordinary skill in the art to replace each of the single transistors MP2 and MP3 of Harston's circuit with a respective compensated transistor switch of the applicant's Fig. 3. Transistors 302b, 304b and 306b would correspond to the first serial combination of respective first compensating, functional MOS, and second compensating transistors, wherein

transistors 302a, 304a and 306a would correspond to the second serial combination of respective first complementary compensating, complementary functional MOS, and second complementary compensating transistors, thus rendering obvious claims 6, 7 and 11. As the applicant admits on page 3, lines 8-28, the use of such compensated switches are conventional/well known means for reducing charge injection of switches in analog circuits. Since Harston's circuit in Fig. 3 can be considered a current switch circuit related to an analog circuit, the compensated switch of Fig. 3 would help reduce charge injection within the circuit if that was desired.

Claims 13 and 14 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Harston as applied to respective claim 1 above. As described previously, Fig. 3 of Harston shows a circuit with a transistor switch MP2 (30), pull-down mirror path MP3 (32), current source MP1 (20), and load capacitor 10pf. However, the reference does not clearly show or disclose a pull-up amplifier as recited within claim 13. It would have been obvious to one of ordinary skill in the art to modify the circuit of Fig. 3 by reversing the polarities and transistor types. The reversal of the polarities and transistor types would provide a means for a higher output voltage. The reversal would replace all the PMOS transistors (i.e. MP1, MP2 and MP3) with NMOS transistors. In this case transistor 32 would be coupled between power source CURRENT CELL and the common connection of current source 20 and transistor switch 30. Therefore, transistor 32 could be deemed a pull-up amplifier, rendering claim 13 obvious. Current source 20 would be coupled between ground and one side of transistor switch 30, rendering obvious claim 14.

No claim is allowable. Claims 15-17, and 20 have been canceled.

Response to Arguments

The applicant's arguments filed Nov 14, 2001 have been fully considered but they are not persuasive. The applicant argues: 1) the labeling of the switches on page 7 are correct; 2) the load continuously receives current; 3) Ravon's system has varying currents and limits transient variations; 4) Ravon's current source is not capacitive or produces spikes during switching; 5) the references fail to mention or teach the current level of the current source is equalized; 6) AAPA fails to teach charge injection by a pull-down mirror path and teaches an unsatisfactory circuit for charge injection; 7) the current flow to ground of Harston performs no useful purpose reduction and is not for reducing charge injection; 8) Harston simply changes state of a DAC; and 9) current spikes are produces by a capacitive current source.

1) Although the applicant's comments indicate the labeling of the switches on page 7 are correct, the examiner disagrees. For example, why is "MC" identified as a "switch" on lines 18 and 19, but as a "current source" on line 21? Also, since current flowing through switch (transistor) MC will have minimal loss due to leakage current within the transistor, the current level at the source of MC is considered equal to the current level at its drain. Therefore, how does the description equalize something that is already equal, or substantially equal?

2) The applicant's argument with respect to current flowing to the load when the transistor switch is open fails to comply with 37 CFR 1.111(b) because it amounts to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the

references because it is believed the applicant's own circuits/disclosure do not clearly show/disclose the limitation as recited and presently understood. Also, the arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. The arguments/comments with respect to claims 21 and 22 merely indicate the claims must be read as a whole, and that they are clear. Even the arguments on page 7 of the amendment are confusing. On one line, the applicant cites the claims' limitation "substantially continuously receives said current flowing from said current source", but several lines later only indicates "the load substantially continuously receives current...for a very short time when the current switch initially allows current to flow to a load." In the latter case, is the current from the current source, or is it provided from the voltage stored across capacitor C1 (see Fig. 5)? Also, does this means the current source is switched on? Page 7 of the applicant's amendment indicates the current from the current source flows through the pull-down mirror path to ground when the switch is initially opened. However, the amendment's comments, the specification, and the figures do not show, or clearly disclose, how the current flows to ground through the pull-down mirror path. It is believed amplifier 400 (shown in the applicant's Fig. 5) is an operational amplifier. Therefore, it is not understood how a current will flow into the inverting input – and to ground. Apparently, current IA will flow through transistor MT, and then down to ground through undisclosed circuitry within amplifier 400. One of ordinary skill in the art would

recognize that when current IA flows through switch 430, both load capacitor CL and capacitor C1 will become charged. Once switch 430 is opened, the charges between capacitors CL and C1 will balance out after some initial current flow across resistor R1 to account for the capacitors' voltage difference due to the voltage drop across resistor R1. Since load 440 will maintain a fairly constant voltage, due to the voltage on charged capacitor C1, there will not be a large change in voltage/current when transistor switch 430 is either opened or closed. When switch 430 is closed, current IA is again allowed to flow to load 440. The voltage held on capacitor C1 will reduce charge injection to the load. However, the current associated with resistor R1 and capacitor C1 is not the current IA from the current source as the claims 21 and 22 clearly recite. Therefore, the current flowing to the load after the switch opens, as recited within some claims, is questionable and clarification is required. [It is noted that the examiner does not equate ground to the load. The examiner maintains the cited references clearly show an alternative current path for the current from the current source to flow through when the transistor switch is open. Therefore, the alternate current path helps maintain a constant current flow from the current source, even when the transistor switch is open.] Thus, after considering the claim limitations and the applicant's figures, clarification is still required which clearly explains how current from the current source can flow to the load when the switching transistor is open as recited within the claims.

3) The applicant argues Ravon's system has varying currents and limits transient variations. Ravon discloses current I is constant, or at least substantially constant (e.g. see column 3, lines 29-31). Therefore, it will have minimal, or no abrupt changes. Also,

by limiting abrupt changes in voltage transitions, abrupt changes in current (and therefore, charge injection) within the circuit is also limited. Due to the known relationships between voltage and current (charge injection), this limitation of transient variations can be considered a reduction in charge injection. For example, limited variations relates to reduced variations.

4) In response to the applicant's argument that Ravon fails to show certain features of the applicant's invention, it is noted that the features upon which the applicant relies (i.e., current source is capacitive and produces current spikes during switching) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). It should also be pointed out that it is not clear what the applicant means by "Ravon's current source is not taught as even being capacitive, and producing current spikes during switching." This appears to imply the applicant's current source is capacitive, and the current source itself might be switched on and off. Since the applicant's and Ravon's current source each comprise a MOS transistor, it is believed both will have a capacitive quality (e.g. gate capacitance). Therefore, the examiner requests to know where these are clearly disclosed in the specification and how the applicant's current source would be capacitive, wherein Ravon's MOS transistor would not be. Also, it is believed the applicant's current source itself is not switched. However, its output current is switched from one current path to another. This will allow the current source to always provide a current flow while the circuit is in operation (e.g. powered up).

5) The applicant's arguments with respect to equalized current level fails to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. For example, none of the claims clearly describe what is meant by equalized current level. If a current source provides substantially a constant current out, couldn't its current be considered substantially equal to the desired or required current the circuit needs? Also, if the current is alternately switched to flow through one of two current paths, wouldn't the current that flows in one path be equal to the current that flows through the other path when it is selected? If not, where would the difference in current level go?

6) In response to the applicant's arguments against the references of Ravon (or Harston) and AAPA individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As the applicant admits on page 3 of the specification, Prior Art Fig. 3 is "Another conventional technique to reduce charge reduction in a current switch circuit." The references doesn't have to specifically teach charge injection by a pull-down mirror path. The applicant shows (and discloses) a single switch can be replaced with the known compensated transistor switch (see Prior Art Fig. 3 and its description). However, it appears the applicant can replace a single switch with the compensated transistor switch within a circuit, but it would not be obvious to anyone else. The examiner disagrees. Ravon shows two single transistors

M1 and M2, with M1 being deemed a transistor switch and M2 being deemed part of a pull-down mirror path in parallel with the transistor switch. Since current I will flow through either M1 or M2 when the respective transistor is conducting, that current flow can be considered equal. For example, if M1 is off, current I will flow through M2, and vice versa. Therefore, the circuit of Ravon is one type of a current switch circuit. If more reduction in charge injection is desired within that type of current switch circuit, why wouldn't it be obvious to one of ordinary skill in the art to replace each of the two single transistors M1 and M2 in Ravon's circuit by the known Prior Art compensated transistor switch? Applying similar reasoning, each of the two single transistors of Harston could be replaced with a respective compensated transistor switch. [Also, it is noted that it appears peculiar that the applicant cites "AAPA teaches an unsatisfactory circuit for reducing charge injection...a compensating switch" (see page 10 of the amendment), but then turns around and uses it to replace a transistor within the invention. Therefore, clarification between the applicant's acceptable compensating switch and AAPA's unsatisfactory circuit is requested. For example, perhaps the applicant only means the AAPA compensating switch is unsatisfactory when it is used by itself.]

7) The applicant comments that the current flow to ground of Harston performs no useful purpose and it is not for reducing charge injection. It appears the applicant requires the prior art reference(s) to specifically cite equal current levels, charge injection, and its reduction. If the reference does not cite a specific term or function, then the examiner is merely reading features into the references that are not taught. However, one of ordinary skill in the art does not require those specific teachings. For

example, one of ordinary skill in the art would realize that current would always be flowing through Harston's current source 20 when it is in operation. The current would flow through whichever one of transistors 30 or 32 would be conducting at the time. For example, if 30 was on, 32 would be off due to their respective gate signals DATAB and DATA, and current would flow through 30. Therefore, the current flow from current source 20 would not have to be restarted or switched on (i.e. from no current flow to the desired flow) during normal operation, and thus the charge injection from current source 20 to the load would be reduced because there would be no (significant) current surge from the current source itself. The current, which would be continuously flowing, would be switched between one current path to ground, and one current path to the load.

8) The applicant argues that Harston simply changes state of a DAC. However, that is considered immaterial to the presently recited claims. The Fig. 3 circuit of Harston is described as a current cell, and it shows a current source, a transistor switch, and what can be deemed a pull-down mirror path. Due to its operations/functions as described previously, the limitations recited within the claims are met. One of ordinary skill in the art would know Harston's current cell could be called a current source switching circuit, and it could be used in other circuits, besides a DAC, that would require switched current when necessary.

9) The applicant also argues that current spikes are produced by a capacitive current source when the current source is switched on. However, as presently understood, the applicant's own current source 420, Ravon's current source 11, and Harston's current source 20 all appear to remain on once their respective circuitry is

placed into operation. Therefore, each current source would continuously provide a current to one of two selected current paths. None of the current sources appear to be turned on and off during normal operation, and thus they would not provide associated spikes related to their switching. Also, each current source is shown as comprising at least one MOS transistor. Therefore, it is believed each current source would have at least some type of capacitive quality (e.g. gate capacitance) related to their structure.

It is believed the rejections and the interpretations related to the circuits and their functions as described above, as well as the comments with respect to the applicant's arguments/comments, are proper.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE
Terry L. Englund
20 December 2001

Kenneth B. Wells
Primary Examiner